74HC595 SPECIFICATION

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

DESCRIPTION

The 74HC595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC595 is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_CP input. The data in each register is transferred to the storage register on a positive-going transition of the ST_CP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages.The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the outputwhenever the output enable input (OE) is LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC	74VIC	
tPHL/tPLH	propagation delay	C_L = 50 pF; V_{CC} = 4.5 V			
	SH_CP to Q7'		19	25	Ns
	SH_CP to Qn		20	24	Ns
	MR to Q7'		100	52	Ns
f_{max}	maximum clock frequency SH_CP and ST_CP		100	57	Mhz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	115	130	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC2} \times f_i \times N + \Sigma(C_L \times V_{CC2} \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. For 74HC595 the condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT					OUTPUT		FUNCTION
SH_CP	**ST_CP**	**OE**	**MR**	**DS**	**Q7'**	**Qn**	a LOW level on MR only affects the shift registers
X	X	L	L	X	L	n.c.	empty shift register loaded into storage register
X		L	L	X	L	L	shift register clear; parallel outputs in high-impedance OFF-state
X	X	H	L	X	L	Z	logic high level shifted into shift register stage 0; contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6') appears on the serial output (Q7')
↑	X	L	H	H	Q6'	n.c.	contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages
X	↑	L	H	X	n.c.	Qn'	contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6'	Qn'	contents of shift register shifted through; previouscontents of the shift register is transferred to the storage register and the parallel output stages

Note

1. H = HIGH voltage level;

L = LOW voltage level;

↑ = LOW-to-HIGH transition;

↓ = HIGH-to-LOW transition;

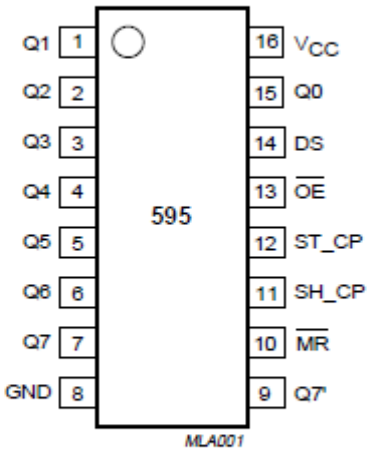
Z = high-impedance OFF-state;

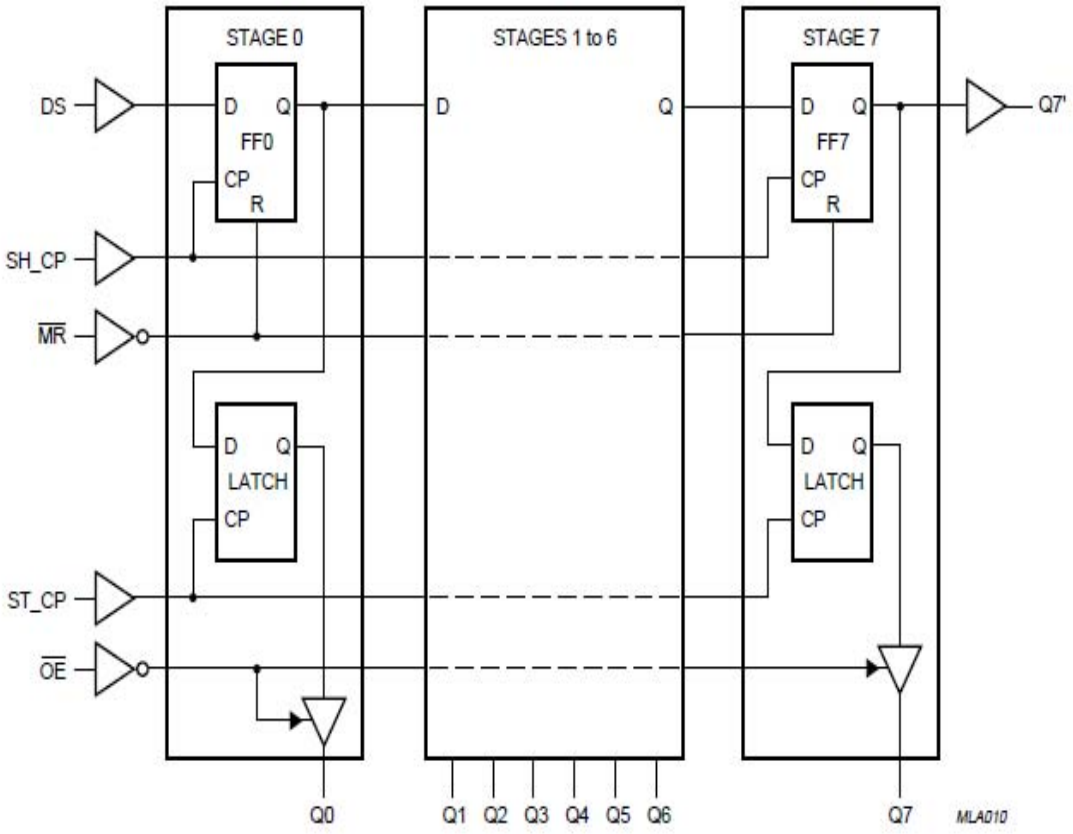
n.c. = no change;

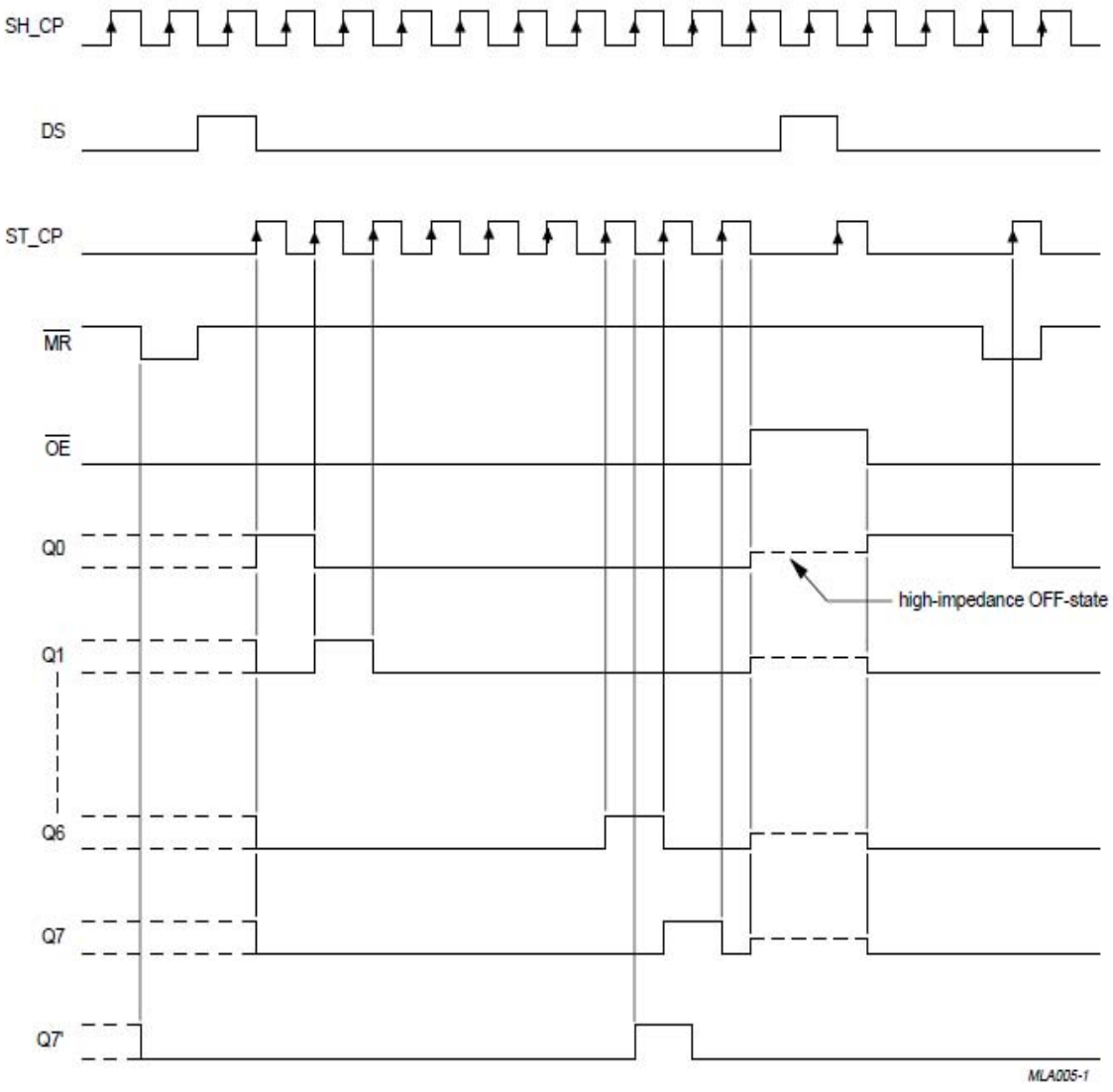
X = don't care.

PINNING

PIN	SYMBOL	DESCRIPTION
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0 V)
9	Q7’	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SH_CP	shift register clock input
12	ST_CP	storage register clock input
13	$\overline{OE}$	output enable (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	VCC	positive supply voltage







RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC			
			MIN.	TYP.	MAX.	UINT
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	Ambient temperature		−40	-	+125	°C
t_r, t_f	input rise and fall time	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns

LIMITED VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.5	+7.0	V
I_{IK}	input diode current	V_I < −0.5 V to V_I > V_{CC} + 0.5 V	–	±20	mA
I_{OK}	Output diode current	V_O < −0.5 V to V_O > V_{CC} + 0.5 V	–	±20	mA
I_O	output source or sink current	V_O = −0.5 V to V_{CC} + 0.5 V			
		Q7' standard output	–	±25	mA
		Qn bus driver outputs	–	±35	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±70	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	power dissipation	T_{amb} = −40 to +125 °C; note 1	–	500	mW

DC CHARACTERISTICS

Type VIC74HC

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

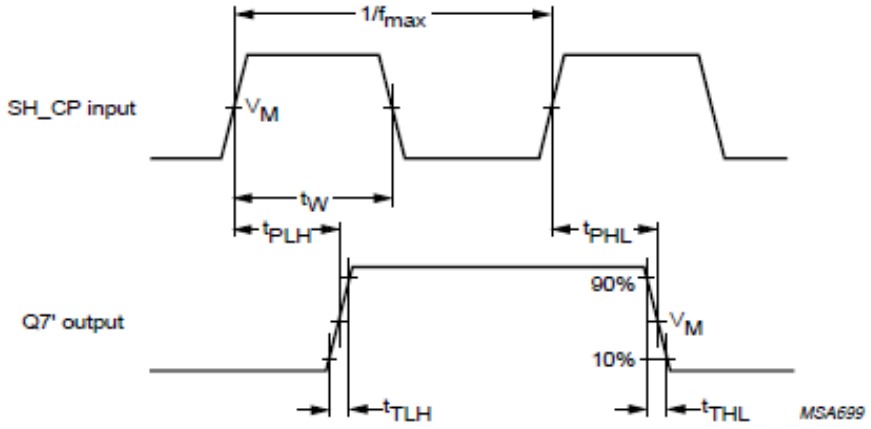
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	-	V
			4.5	3.15	2.4	-	V
			6.0	4.2	3.2	-	V
V_{IL}	LOW-level input voltage		2.0	-	0.8	0.5	V
			4.5	-	2.1	1.35	V
			6.0	-	2.8	1.8	V
V_{OH}		V_I = V_{IH} or V_{IL}					
		all outputs					
		I_O = −20 μA	2.0	1.9	2.0	-	V
			4.5	4.4	4.5	-	V
			6.0	5.9	6.0	-	V
		Q7'standard output					
		I_O = −4.0 Ma	4.5	3.84	4.32	-	V
		I_O = −5.2 mA	6.0	5.34	5.81	-	V
		Qn bus driver outputs					
		I_O = −6.0 mA	4.5	3.84	4.32	-	V
		I_O = −7.8 mA	6.0	5.34	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs					
		I_O = 20 μA	2.0	-	0	0.1	V
			4.5	-	0	0.1	V
			6.0	-	0	0.1	V
		Q7' standard output					
		I_O = 4.0 mA	4.5	-	0.15	0.33	V
		I_O = 7.8 mA	6.0	-	0.16	0.33	V
		Qn bus driver outputs					
		I_O = 6.0 mA	4.5	-	0.16	0.33	V
		I_O = 7.8 mA	6.0	-	0.16	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	-	-	±1.0	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	6.0	-	-	±5.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	-	-	80	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	Vcc (V)				
Tamb = −40 to +125 °C							
VIH	HIGH-level input voltage		2.0	1.5	-	-	V
			4.5	3.15	-	-	V
			6.0	4.2	-	-	V
VIL	LOW-level input voltage		2.0	-	-	0.5	V
			4.5	-	-	1.35	V
			6.0	-	-	1.8	V
VOH	HIGH-level output voltage	VI = VIH or VIL					
		all outputs					
		IO = −20 μA	2.0	1.9	-	-	V
			4.5	4.4	-	-	V
			6.0	5.9	-	-	V
		Q7' standard output					
		IO = −4.0 mA	4.5	3.7	-	-	V
		IO = −5.2 mA	6.0	5.2	-	-	V
		Qn bus driver outputs					
		IO = −6.0 mA	4.5	3.7	-	-	V
		IO = −7.8 mA	6.0	5.2	-	-	V
VOL	LOW-level output voltage	VI = VIH or VIL					
		all outputs					
		IO = 20 μA	4.5	-	-	0.1	V
		Q7' standard output					
		IO = 4.0 mA	4.5	-	-	0.4	V
		Qn bus driver outputs					
		IO = 6.0 mA	4.5	-	-	0.4	V
ILI	inputleakage current	VI = VCC or GND	5.5	-	-	±1.0	μA
IOZ	3-state output OFF-state current	VI = VIH or VIL; VO = VCC or GND	5.5	-	-	±10.0	μA
ICC	quiescent supply current	VI = VCC or GND; IO = 0	5.5	-	-	160	μA

Note

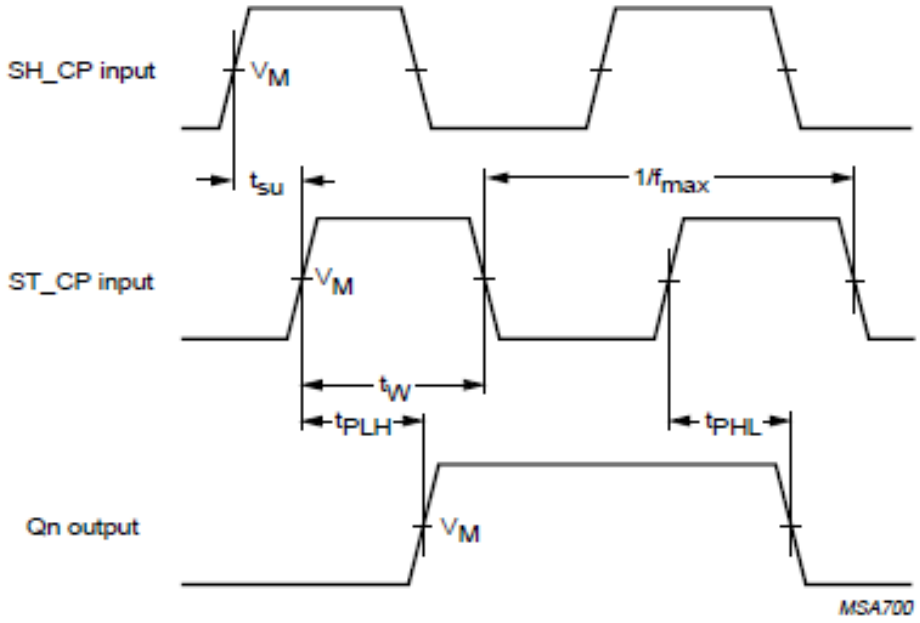
1. All typical values are measured at Tamb = 25 °C.

AC WAVEFORMS



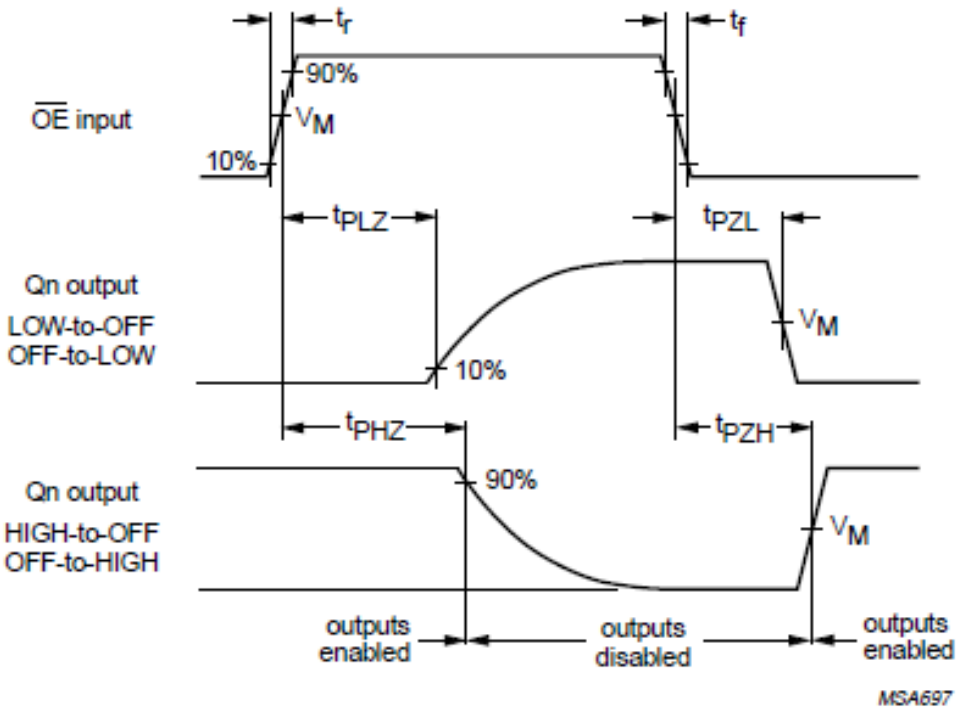
74HC595: VM = 50%; VI = GND to VCC.

Waveforms showing the data set-up and hold times for the DS input.



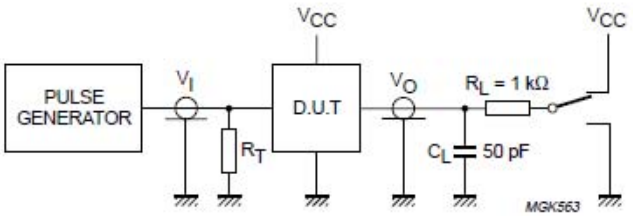
74HC595: VM = 50%; VI = GND to VCC.

Waveforms showing the Master Reset (MR) pulse width, the master reset to output (Q7') propagationdelay and the master reset to shift clock (SH_CP) removal time.



74HC595: VM = 50%; VI = GND to VCC.

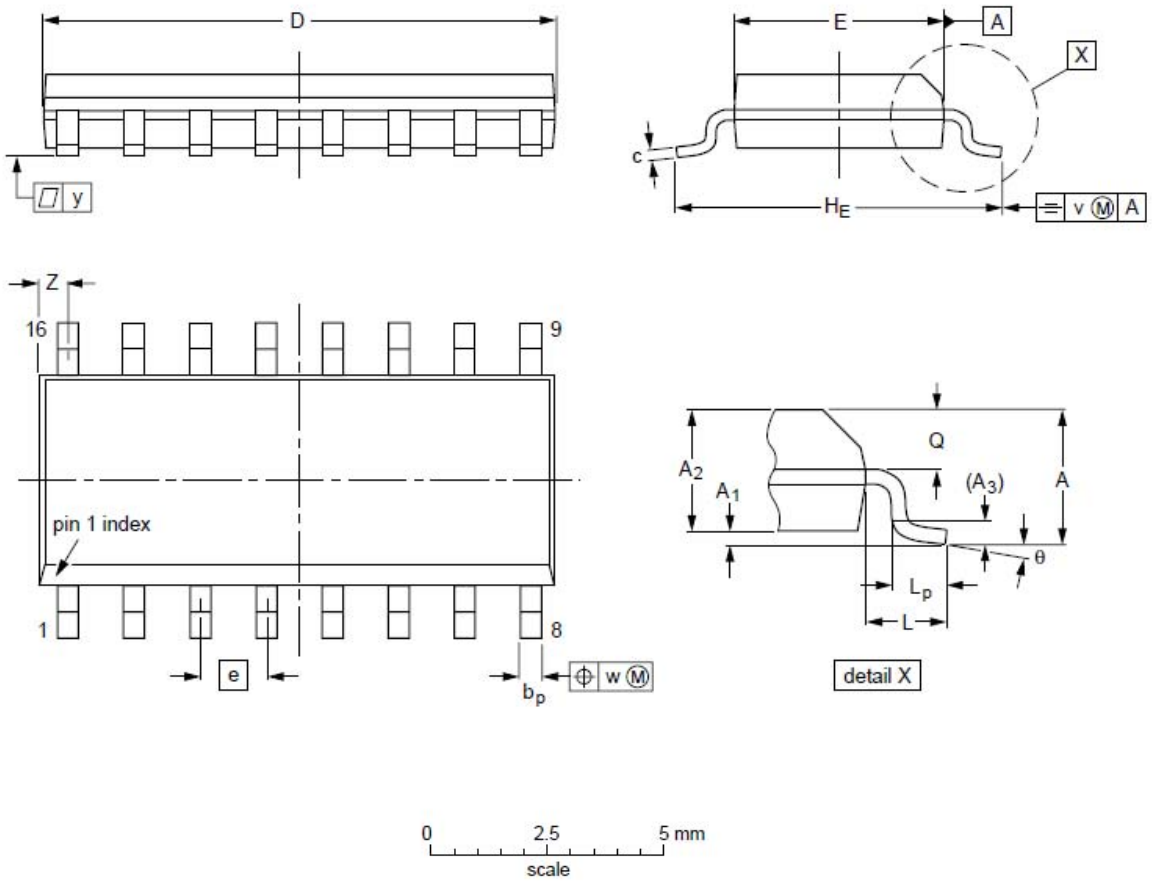
Waveforms showing the 3-state enable and disable times for input OE.



TEST	SWITCH
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

SO16: plastic small outline package; 16 leads; body width 3.9 mm



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

