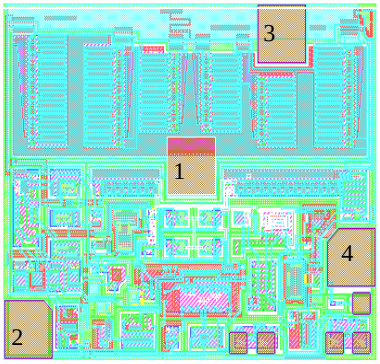
CHIP APPEARANCE	CHIP SIZE			1,6 × 2,0 mm
	CHIP THICKNESS			460 ± 30 μm (or 280 ± 30 μm)
	BONDING PAD DIMENSION	1	INPUT	240 × 240 μm
		2	OUTPUT	240 × 240 μm
		3	OUTPUT	240 × 240 μm
		4	ADJ	240 × 240 μm
	SCRIBE LINE WIDTH			80 μm
	TOP METAL			AlSi
	BACK METAL			– (or Ti-Ni(V)-Ag)
	WAFER SIZE			100 mm

ABSOLUTE MAXIMUM RATINGS OVER OPERATING TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

	LM317	UNIT
Input-to-output differential voltage, V_I - Vo	40	V
Continuous total dissipation at 25 °C free-air temperature	2	W
Continuous total dissipation at (or below) 25 °C case temperature	15	W
Operating free-air, case, or virtual junction temperature range	0 to 125	°C
Storage temperature range	-65 to 150	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260	°C

RECOMMENDED OPERATING CONDITIONS

	LM317		UNIT
	MIN	MAX	
Output current, I_O	10	1500	mA
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics over recommended ranges of operating virtual junction temperature

(unless otherwise noted) (see Note 1)

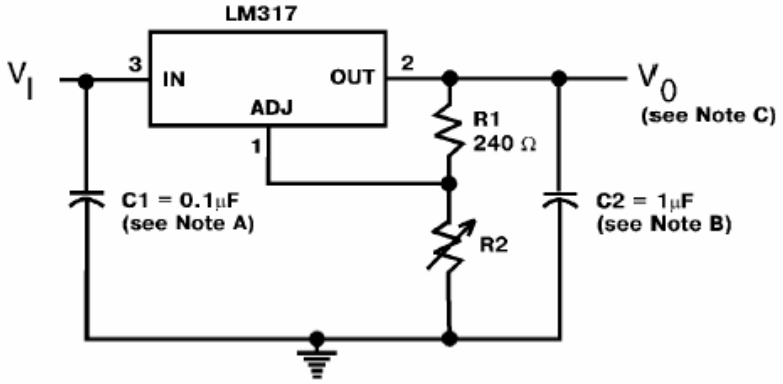
PARAMETER	TEST CONDITIONS*		LM317			UNIT
			MIN	TYP	MAX	
Input regulation (See Note 2)	V_I-V_O=3 V to 40 V,	TJ = MIN to MAX		0.01	0.04	%/ V
	(See Note 3)	I_O = 10 mA to 1.5 A		0.02	0.07	
Ripple rejection	Vo=10 V, f=120 Hz			65		dB
	Vo=10 V, f=120 Hz 10-μF capacitor between ADJ and ground		66	80		
Output regulation	Io = 10 mA to 1.5 A,	Vo ≤5 V		5	25	mV
	T_J= 25 °C, (See Note 3)	Vo > 5 V		0.1	0.5	%
	Io = 10 mA to 1.5 A,	Vo ≤ 5 V		20	70	mV
	(See Note 3)	Vo > 5 V		0.3	1.5	%
Output voltage change with temperature	T_J = MIN to MAX			1		%
Output voltage long-term drift (see Note 4)	After 1000 h at T_J = MAX and V_I-Vo =40 V			0.3	1	%
Output noise voltage	f= 10 Hz to 10 kHz, T_J =25°C			0.003		%
Minimum output current to maintain regulation	V_I-Vo = 40 V			3.5	10	mA
Peak output current	V_I-Vo ≤ 15 V		1.5	2.2		A
	V_I-Vo ≤ 40 V, T_J =25°C		0.15	0.4		
Adjustment-terminal current				50	100	μA
Change in adjustment-terminal current	V_I-Vo=2.5 V to 40 V, Io = 10 mA to 1.5 A			0.2	5.0	μA
Reference voltage (output to ADJ)	V_I-Vo = 3 V to 40 V, Io=10 mA to 1.5 A, P ≤ 15W		1.2	1.25	1.3	V

* Unless otherwise noted, these specifications apply for the following test conditions: V_I - V_O = 5V and I_O = 0.5 A. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES:

1. All characteristics are measured with a 0.1 - μF capacitor across the input and a 1 - μF capacitor across the output.
2. Input regulation is expressed here as the percentage change in output voltage per 1 - V change at the input.
3. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
4. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL APPLICATION DATA



NOTES:
A. Use of an input bypass capacitor is recommended if regulator is far from filter capacitors.
B. Use of an output capacitor improves transient response but is optional

C. Output voltage is calculated from the equation : $V_0 = V_{ref}\left(1+\frac{R_2}{R_1}\right)$

V_{ref} equals the difference between the output and adjustment terminal voltages

Probing spec (Ta = 25°C) chips on wafer

№	Name (Mode)	Limit			Condition		
		MIN	MAX	UNIT	INPUT	GROUND	OUTPUT
1	Input current	- 85.0	-	uA	22 V	0 V	-10 uA
2	Reference voltage (output to ADJ)	1,225	1,275	V	45 V		- 9 mA
3					45 V		-50 mA
4					42 V		- 50 mA
5					42 V		- 9 mA
6					4 V		- 9 mA
7					4 V 30 V		- 200 mA - 200 mA